Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1-17. (Canceled)

18. (Withdrawn) An integrated circuit comprising:

a CMOS circuit;

an n-channel field effect transistor and a p-channel field effect transistor in the CMOS circuit;

said n-channel field effect transistor comprising:

a crystalline semiconductor formed on an insulating surface;

a source region, a drain region and a channel forming region in the crystalline semiconductor;

a gate insulating film;

a gate electrode formed over the channel forming region;

said channel forming region comprising:

a plurality of carrier moving regions;

a plurality of impurity regions,

wherein the plurality of impurity region of the channel forming region are formed locally for pinning of a depletion layer,

wherein the depletion layer is formed from the drain region toward the channel forming region and the source region,

wherein each of the impurity regions comprises an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed.

19. (Withdrawn) An integrated circuit comprising:

a memory circuit;

a field effect transistor in the memory circuit;

said field effect transistor comprising:

a crystalline semiconductor;

a source region, a drain region and a channel forming region in the crystalline semiconductor;

a gate insulating film;

a gate electrode formed over the channel forming region;

said channel forming region comprising:

a plurality of carrier moving regions;

a plurality of impurity regions;

wherein the plurality of the impurity region in the channel forming region are formed locally for pinning of a depletion layer,

wherein the depletion layer is formed from the drain region toward the channel forming region and the source region,

wherein each of the impurity regions comprises an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed.

20. (Withdrawn) An integrated circuit according to claim 18, wherein the impurity element is for forming a built-in potential difference locally in the channel forming region.

21. (Withdrawn) An integrated circuit according to claim 19, wherein said impurity element belongs to group XIII.

22. (Withdrawn) An integrated circuit according to claim 21, wherein said impurity element is boron.

23. (Withdrawn) An integrated circuit according to claim 18, wherein the impurity element belongs to group XV.

24. (Withdrawn) An integrated circuit according to claim 23, wherein said impurity element is phosphorus or arsenic.

25. (Withdrawn) An integrated circuit according to claim 18, wherein the carrier moving regions are intrinsic or substantially intrinsic.

26. (Withdrawn) An integrated circuit according to claim 25, wherein said substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $2 \times 10^{18}$ atoms/cm$^3$.

27. (Withdrawn) An integrated circuit according to claim 25, wherein said substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $1 \times 10^{17}$ atoms/cm$^3$.

28. (Withdrawn) An integrated circuit according to claim 18, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

29. (Withdrawn) An integrated circuit according to claim 18, wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a

channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

30. (Withdrawn) An integrated circuit according to claim 18, wherein a reduction in threshold voltage caused by a short channel effect occurring in the channel forming region during driving is compensated by an increase in threshold voltage caused by a narrow channel effect obtained by utilizing the impurity regions.

31. (Withdrawn) An integrated circuit according to claim 18, wherein the impurity regions serve as regions for buffering stress that occurs in the crystalline semiconductor.

32. (Withdrawn) An integrated circuit according to claim 18, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

33. (Withdrawn) An integrated circuit according to claim 18, wherein the impurity regions have dot patterns.

34. (Withdrawn) An integrated circuit according to claim 18, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

35. (Withdrawn) An integrated circuit according to claim 18, wherein a threshold voltage is controlled by controlling widths of the carrier moving regions.

36. (Withdrawn) An integrated circuit according to claim 18, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

37. (Withdrawn) The integrated circuit of claim 18 in combination with at least an electric apparatus selected from the group consisting of a liquid crystal display device, an EL

display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

38. (Canceled)

39. (Withdrawn) An EL device having the integrated circuit according to claim 18.

40. (Withdrawn) An EL device having the integrated circuit according to claim 19.

41. (Withdrawn) An integrated circuit according to claim 19, wherein the impurity element is for forming a built-in potential difference locally in the channel forming region.

42. (Withdrawn) An integrated circuit according to claim 19, wherein the impurity element belongs to group XV.

43. (Withdrawn) An integrated circuit according to claim 42, wherein the impurity element is phosphorus or arsenic.

44. (Withdrawn) An integrated circuit according to claim 19, wherein the carrier moving regions are intrinsic or substantially intrinsic.

45. (Withdrawn) An integrated circuit according to claim 44, wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $2 \times 10^{18}$ atoms/cm$^3$.

46. (Withdrawn) An integrated circuit according to claim 44, wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than $5 \times 10^{15}$ atoms/cm$^3$ and an oxygen concentration is less than $1 \times 10^{17}$ atoms/cm$^3$.

47. (Withdrawn) An integrated circuit according to claim 19, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

48. (Withdrawn) An integrated circuit according to claim 19, wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

49. (Withdrawn) An integrated circuit according to claim 19, wherein a reduction in threshold voltage caused by a short channel effect occurring in the channel forming region during driving is compensated by an increase in threshold voltage caused by a narrow channel effect obtained by utilizing the impurity regions.

50. (Withdrawn) An integrated circuit according to claim 19, wherein the impurity regions serve as regions for buffering stress that occurs in the crystalline semiconductor.

51. (Withdrawn) An integrated circuit according to claim 19, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

52. (Withdrawn) An integrated circuit according to claim 19, wherein the impurity regions have dot patterns.

53. (Withdrawn) An integrated circuit according to claim 19, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

54. (Withdrawn) An integrated circuit according to claim 19, wherein a threshold voltage is controlled by controlling widths of the carrier moving regions.

55. (Withdrawn) An integrated circuit according to claim 19, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

56. (Withdrawn) The integrated circuit of claim 19 in combination with at least an electric apparatus selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

57. (Canceled)

58. (Previously Presented) A semiconductor device having a Bi-CMOS circuit comprising;

a first layer comprising at least one bipolar transistor;

a second layer comprising at least one n-channel transistor and one p-channel transistor over the first layer;

wherein each of the n-channel transistor and the p-channel transistor comprises;

a semiconductor layer comprising:

a channel forming region;

a source region; and

a drain region;

a gate insulating film; and

a gate electrode.

59. (Withdrawn) A semiconductor device having a DRAM circuit comprising:

a first layer comprising at least one capacitor comprising:

a first electrode;

a second electrode; and

an insulating film between the first and the second electrode;

a second layer comprising at least one transistor over the first layer;

wherein the transistor comprises:

a semiconductor layer comprising:

a channel forming region;

a source region; and

a drain region; and

a gate electrode.

60. (Withdrawn) A semiconductor device having a SRAM circuit comprising:

a first layer comprising one first transistor;

a second layer comprising one second transistor over the first layer;

a third layer comprising one third transistor over the third layer;

wherein each of the first, second and third transistors comprises:

a channel forming region;

a source region;

a drain region;

a gate insulating film; and

a gate electrode.

61. (Currently Amended) A semiconductor device having a stacked CMOS circuit comprising:

a first layer comprising at least one first transistor;

a second layer comprising at least one second transistor over the first layer;

wherein each of the first and second transistors comprises:

a channel forming region;

a source region;

a drain region; and

a gate electrode,

wherein the first transistor is an n-channel transistor and the second transistor is a p-channel transistor,

wherein a plurality of first impurity regions each comprising a semiconductor material and [[an]] a first impurity element are included at least in the channel forming region of the first transistor,

wherein a plurality of second impurity regions each comprising a semiconductor material and a second impurity element are included at least in the channel forming region of the second transistor,

wherein each of the plurality of first impurity regions is formed in a part of the channel forming region in the first transistor,

wherein each of the plurality of second impurity regions is formed in a part of the channel forming region in the second transistor,

wherein the first impurity element belongs to group 13 and the second impurity element belongs to group 15.

62. (Previously Presented) A semiconductor device having a Bi-CMOS circuit comprising;

at least one bipolar transistor;

an insulating film over the at least one bipolar transistor; and

at least one n-channel transistor and one p-channel transistor over the insulating film;

wherein each of the n-channel transistor and the p-channel transistor comprises:

a semiconductor layer comprising:

a channel forming region;

a source region; and

a drain region;

a gate insulating film; and

a gate electrode;

wherein a plurality of impurity regions each comprising a semiconductor material and an impurity element are included at least in the channel forming region,

wherein each of the plurality of impurity regions is formed in a part of the channel forming region.

63. (Withdrawn) A semiconductor device having a DRAM circuit comprising:

a first layer comprising at least one capacitor comprising:

a first electrode;

a second electrode; and

an insulating film between the first and the second electrode;

a second layer comprising at least one transistor over the first layer;

wherein the transistor comprises:

a semiconductor layer comprising:

a channel forming region;

a source region; and

a drain region; and

a gate electrode;

wherein a plurality of carrier moving regions and a plurality of impurity regions comprise an impurity element are included at least in the channel forming region.

64. (Withdrawn) A semiconductor device having a SRAM circuit comprising:

a first layer comprising one first transistor;

a second layer comprising one second transistor over the first layer;

a third layer comprising one third transistor over the third layer;

wherein each of the first, second and third transistors comprises:

a channel forming region;

a source region;

a drain region;

a gate insulating film; and

a gate electrode;

wherein a plurality of carrier moving regions and a plurality of impurity regions comprise an impurity element are included at least in the channel forming region.

65. (Canceled)

66. (Previously Presented) An electric apparatus comprising the semiconductor device according to claim 58, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

67. (Withdrawn) An electric apparatus comprising the semiconductor device according to claim 59, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

68. (Withdrawn) An electric apparatus comprising the semiconductor device according to claim 60, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

69. (Previously Presented) An electric apparatus comprising the semiconductor device according to claim 61, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

70. (Previously Presented) An electric apparatus comprising the semiconductor device according to claim 62, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

71. (Withdrawn) An electric apparatus comprising the semiconductor device according to claim 63, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

72. (Withdrawn) An electric apparatus comprising the semiconductor device according to claim 64, wherein the electric apparatus is selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a

car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

73. (Canceled)

74. (Previously Presented) An EL device having the semiconductor device according to claim 58.

75. (Withdrawn) An EL device having the semiconductor device according to claim 59.

76. (Withdrawn) An EL device having the semiconductor device according to claim 60.

77. (Previously Presented) An EL device having the semiconductor device according to claim 61.

78. (Previously Presented) An EL device having the semiconductor device according to claim 62.

79. (Withdrawn) An EL device having the semiconductor device according to claim 63.

80. (Withdrawn) An EL device having the semiconductor device according to claim 64.

81. (Canceled)

82. (Previously Presented) A semiconductor device according to claim 58, wherein the semiconductor layer comprises single crystal silicon.

83. (Withdrawn) A semiconductor device according to claim 59, wherein the semiconductor layer comprises single crystal silicon.

84. (Withdrawn) A semiconductor device according to claim 60, wherein the channel forming region, source region and drain region comprise single crystal silicon.

85. (Previously Presented) A semiconductor device according to claim 61, wherein the channel forming region, source region and drain region comprise single crystal silicon.

86. (Previously Presented) A semiconductor device according to claim 62, wherein the semiconductor layer comprises single crystal silicon.

87. (Withdrawn) A semiconductor device according to claim 63, wherein the semiconductor layer comprises single crystal silicon.

88. (Withdrawn) A semiconductor device according to claim 64, wherein the channel forming region, source region and drain region comprise single crystal silicon.

89. (Canceled)

90. (Previously Presented) A semiconductor device according to claim 58, wherein the second layer has a SOI structure.

91. (Withdrawn) A semiconductor device according to claim 59, wherein the second layer has a SOI structure.

92. (Withdrawn) A semiconductor device according to claim 60, wherein the second and third layers have a SOI structure.

93. (Previously Presented) A semiconductor device according to claim 61, wherein the second layer has a SOI structure.

94. (Previously Presented) A semiconductor device according to claim 62, wherein the second layer has a SOI structure.

95. (Withdrawn) A semiconductor device according to claim 63, wherein the second layer has a SOI structure.

96. (Withdrawn) A semiconductor device according to claim 64, wherein the second and third layers have a SOI structure.

97. (Canceled)

98. (Previously Presented) A semiconductor device according to claim 62, wherein the impurity element belongs to group 13.

99. (Withdrawn) A semiconductor device according to claim 63, wherein the impurity element belongs to group 13.

100. (Withdrawn) A semiconductor device according to claim 64, wherein the impurity element belongs to group 13.

101. (Currently Amended) A semiconductor device according to claim [[97]] 61, wherein the first impurity element is boron.

102. (Previously Presented) A semiconductor device according to claim 98, wherein the impurity element is boron.

103. (Withdrawn) A semiconductor device according to claim 99, wherein the impurity element is boron.

104. (Withdrawn) A semiconductor device according to claim 100, wherein the impurity element is boron.

105. (Canceled)

106. (Previously Presented) A semiconductor device according to claim 62, wherein the impurity element belongs to group 15.

107. (Withdrawn) A semiconductor device according to claim 63, wherein the impurity element belongs to group 15.

108. (Withdrawn) A semiconductor device according to claim 64, wherein the impurity element belongs to group 15.

109. (Currently Amended) A semiconductor device according to claim [[105]] 61, wherein the second impurity element is phosphorus or arsenic.

110. (Previously Presented) A semiconductor device according to claim 106, wherein the impurity element is phosphorus or arsenic.

111. (Withdrawn) A semiconductor device according to claim 107, wherein the impurity element is phosphorus or arsenic.

112. (Withdrawn) A semiconductor device according to claim 108, wherein the impurity element is phosphorus or arsenic.

113. (Currently Amended) A semiconductor device according to claim 61, wherein a width W of the channel forming region, a total width $W_{pi}$ of the first or second impurity regions, and a total width $W_{pa}$ of regions between the first or second impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

114. (Previously Presented) A semiconductor device according to claim 62, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

115. (Withdrawn) A semiconductor device according to claim 63, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

116. (Withdrawn) A semiconductor device according to claim 64, wherein a width W of the channel forming region, a total width $W_{pi}$ of the impurity regions, and a total width $W_{pa}$ of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

117. (Currently Amended) A semiconductor device according to claim 61, wherein a total width of regions other than the first or second impurity regions in the channel forming region is within a range of 30 to 3,000 Å.

118. (Previously Presented) A semiconductor device according to claim 62, wherein a total width of regions other than the impurity regions in the channel forming region is within a range of 30 to 3,000 Å.

119. (Withdrawn) A semiconductor device according to claim 63, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

120. (Withdrawn) A semiconductor device according to claim 64, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

121. (Currently Amended) A semiconductor device according to claim 61, wherein the first or second impurity regions have dot patterns.

122. (Previously Presented) A semiconductor device according to claim 62, wherein the impurity regions have dot patterns.

123. (Withdrawn) A semiconductor device according to claim 63, wherein the impurity regions have dot patterns.

124. (Withdrawn) A semiconductor device according to claim 64, wherein the impurity regions have dot patterns.

125. (Currently Amended) A semiconductor device according to claim 61, wherein the first or second impurity regions have linear patterns substantially parallel with a channel direction.

126. (Previously Presented) A semiconductor device according to claim 62, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

127. (Withdrawn) A semiconductor device according to claim 63, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

128. (Withdrawn) A semiconductor device according to claim 64, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

129. (Currently Amended) A semiconductor device according to claim 61, wherein the first or second impurity element in the first or second impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

130. (Previously Presented) A semiconductor device according to claim 62, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.

131. (Canceled)

132. (Canceled)

133. (Previously Presented) A semiconductor device according to claim 61, further comprising a plurality of carrier moving regions comprising a semiconductor material.

134. (Previously Presented) A semiconductor device according to claim 62, further comprising a plurality of carrier moving regions comprising a semiconductor material.

135. (New) A semiconductor device having a stacked CMOS circuit comprising:
a first layer comprising at least one first transistor;
a second layer comprising at least one second transistor over the first layer;
wherein each of the first and second transistors comprises:

a channel forming region;

a source region;

a drain region; and

a gate electrode,

wherein the first transistor is a p-channel transistor and the second transistor is an n-channel transistor,

wherein a plurality of first impurity regions each comprising a semiconductor material and a first impurity element are included at least in the channel forming region of the first transistor,

wherein a plurality of second impurity regions each comprising a semiconductor material and a second impurity element are included at least in the channel forming region of the second transistor,

wherein each of the plurality of first impurity regions is formed a part of the channel forming region in the first transistor,

wherein each of the plurality of second impurity regions is formed in a part of the channel forming region in the second transistor,

wherein the first impurity element belongs to group 15 and the second impurity element belongs to group 13.

136. (New) A semiconductor device according to claim 135, wherein the first impurity element is phosphorous or arsenic.

137. (New) A semiconductor device according to claim 135, wherein the second impurity element is boron.

138. (New) A semiconductor device according to claim 135, wherein a width W of the channel forming region, a total width $W_{pi}$ of the first or second impurity regions, and a total

width $W_{pa}$ of regions between the first or second impurity regions satisfy relationships $W_{pi}/W$ = 0.1 to 0.9, $W_{pa}/W$ = 0.1 to 0.9, and $W_{pi}/W_{pa}$ = 1/9 to 9.

139. (New) A semiconductor device according to claim 135, wherein a total width of regions other than the first or second impurity regions in the channel forming region is within a range of 30 to 3,000 Å.

140. (New) A semiconductor device according to claim 135, wherein the first or second impurity regions have dot patterns.

141. (New) A semiconductor device according to claim 135, wherein the first or second impurity regions have linear patterns substantially parallel with a channel direction.

142. (New) A semiconductor device according to claim 135, wherein the first or second impurity element in the first or second impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/$cm^3$.